What is claimed is:

1   1.   A random access memory, comprising:

2   a first memory bank;

3   a second memory bank;

4   an error checking circuit operatively connected to receive data read from the first

5   memory bank; and

6   a multiplexer operatively connected to input data read from both the first memory

7   bank and the second memory bank, wherein input selection of the multiplexer is

8   controlled by an output of the error checking circuit.

1   2.   The random access memory of claim 1, wherein the first memory bank and

2   second memory bank comprise static random access memory.

1   3.   The random access memory of claim 1, wherein the error checking circuit

2   comprises a parity checking circuit.

1   4.   The random access memory of claim 1, wherein when the parity checking circuit

2   determines parity of the data read from the first memory bank is correct, the multiplexer

3   selects the input from the first memory bank, and when the parity checking circuit

4   determines parity of the data read from the first memory bank is incorrect, the

5   multiplexer selects the input from the second memory bank.

1   5.   The random access memory of claim 1, wherein the first memory bank, the

2   second memory bank, the error checking circuit, and the multiplexer are implemented on

3   a single chip.

1   6.   The random access memory of claim 1, further comprising means for writing data

2   simultaneously to the first memory bank and the second memory bank.

1   7.   A partitioned memory system, comprising:

2   a first memory device;

3   a second memory device;

4   means for writing data to the first and second memory devices in parallel;

5   means for error checking data read from the first memory device and outputting a

6   result indicative thereof; and

7   selection means for selecting data read from the first memory device for output to

8   a bus if the result from the error checking means indicates no error and for selecting data

9   read from the second memory device for output to the bus if the result from the error

10 checking means indicates an error.

1   8.   The memory system of claim 7, wherein the first memory device and the second

2   memory device comprise static random access memory.

1   9.   The memory system of claim 7, wherein the error checking means comprises

2   means for checking parity.

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1   10.   The memory system of claim 7, wherein the selection means comprises a

2   multiplexer.

1   11.   The memory system of claim 7, wherein the first memory device, the second

2   memory device, the error checking means, and the selection means are implemented on a

3   single chip.

1   12.   A method for reducing errors in a memory system, comprising:

2   writing data into first and second memory banks of the memory system in

3   parallel;

4   reading data from a desired location of the first memory bank;

5   checking the data read from the first memory bank for errors;

6   if no errors are present, outputting the data read from the first memory bank to a

7   bus; and

8   if the data read from the first memory bank contains errors, outputting data read

9   from a parallel location in the second memory bank to the bus.

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1   13.   The method to claim 12, wherein checking the data read from the first memory

2   bank for errors comprises checking the data for parity

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1   14.   The method of claim 12, wherein the data read from the first memory bank is

2   cleared for parity on a byte-by-byte basis.

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1   15.   The method of claim 12, wherein data from one of the first memory bank and

2   second memory bank are selected using a multiplexer.

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1   16.   A partitioned static random access memory comprising:

2   a first static random access memory bank;

3   a second static random access memory bank, the first and second static random

4   access memory banks being configured such that data may be written to parallel locations

5   therein;

6   a parity checking circuit configured to check parity of data read from the first

7   static random access memory bank and to output a result indicative thereof; and

8   a multiplexer configured to receive data read from the parallel locations in the first and

9   second static random access memory banks and to select one of said data depending upon

10   the result output by the parity checking circuit.